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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,724	02/10/2004	Masatoshi Yasutake	S004-5210	3824

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EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,724	YASUTAKE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 36-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 36-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose, US Patent 6,826,971 (herein referred to as Hirose'971) in view of Chung et al, US Patent 5,604,156.

Regarding claim 1, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a focused ion beam to form a sample chip having a wall surface with stepped potions formed (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), and a third step of

observing a the wall surface of the taken sample chip with a scanning probe microscope (SPM) (column 7, line 55).

Hirose'971 fails to teach the stepped portion is formed due to differences in etching rate of material forming the wall surface.

However, at the time the invention of the instant application was made, it was well known in the art that etching at least two different materials with different etch rates results in a protrusion portion occurring on the surface of an area that is etched. An example of such is shown in Chung, figure 1E and column 2, lines 8-17, which teaches a stepped protrusion "C" occurring on the side wall surface of a trench due to the different etch rates of the semiconductor materials involved.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a stepped portion due to the difference in etching rates of materials forming the wall surface because this is an inherent feature that occurs when the semiconductor materials used have different etch rates.

Claims 36-38, 40, 41, 43, 44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose, US Patent 6,826,971 (referred to as "Hirose'971") in view of Hitachi LTD, Patent Abstract of Japan 05-052,721 (referred to as

"Hitachi") and Mizumura, US Patent 5,825,035 (all as cited in previous office action).

Regarding claim 36, Hirose '971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of picking-up the sample chip from the sample (column 5, line 18-23), and a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55).

Hirose'971 fails to teach a third step of irradiating a wall surface of the sample chip with an argon beam to thereby etch the wall surface.

Hitachi teaches a third step of irradiating a wall surface of the sample chip with a beam to thereby etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis.

Hirose"971 and Hitachi fail to teach the beam is an argon beam.

Mizumura teaches the beam is an argon beam (column 9, lines 26-35), with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971 and Hitachi because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

Regarding claim 37, Mizumura teaches the argon ion beam is irradiated from a tangent direction of the wall surface (figures 32 or figures 42-47).

Regarding claim 38, Hirose'971 teaches the first focused energy beam is a focused ion beam (column 4, line 48).

Regarding claim 40, Hirose'971 teaches a method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, line 18-23), a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), and a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface (to further explain, Hirose'971 teaches one method of observing the sample is through a TEM type of microscope. Hirose'971 explains that if necessary, the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM), and a step of repeating the third to fifth steps a preselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Hirose'971 fails to teach the third step of irradiating a wall surface of the sample chip with an argon ion beam thereby to etch the wall surface.

Hitachi teaches the third step of irradiating a wall surface of the sample chip with a beam thereby to etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis.

Hirose'971 and Hitachi fail to teach the beam is an argon ion beam.

Mizumura teaches the beam is an argon ion beam (column 9, lines 26-35), with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971 and Hitachi because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

Regarding claim 41, Hirose'971 teaches the first focused energy beam is a focused ion beam (column 4, line 48).

Regarding claim 43, Hirose'971 teaches method of preparing a sample chip and observing a wall surface thereof, comprising the steps of a first step of etching a surrounding area of a preselected portion of a sample by irradiating the sample with a first focused energy beam to form a sample chip (the preselected area is the area of the defect **3** and an area surrounding the preselected portion would be everything else on chip **2** and the chip has several wall surfaces formed. See column 4, lines 46 to column 5, line 17), a second step of taking out the sample chip from the sample (column 5, lines 18-23), a fourth step of observing the etched wall surface of the sample chip using a scanning probe microscope (column 7, line 55), a fifth step of irradiating the observed wall surface of the sample chip with the first focused energy beam to thereby to etch the observed wall surface (to further explain, Hirose'971 teaches one method of observing the sample is through a TEM type of microscope. Hirose'971 explains that if necessary,

the sample can be thinned using the focus ion beam. Therefore, one of ordinary skill in the art would know that after a first observation using a TEM or SPM, if the sample is too thick to observe, the sample would need to be thinned, using a FIB and that the sample can be thinned by irradiating the observed wall surface and/or any wall surface that is deemed necessary, then observing the sample again using a TEM or SPM) and a step of repeating the fourth and fifth steps a reselected number of times (which can be done by repeat observing and irradiating to thin down the sample).

Hirose'971 fails to teach a third step of irradiating a wall surface of the sample chip with an argon ion beam to thereby to etch the wall surface.

Hitachi teaches teach a third step of irradiating a wall surface of the sample chip with a beam thereby to etch the wall surface (abstract, [0018]) first, as a means of forming a separated sample directly after the formation of an FIB etched sample, which can be inserted into various kinds of analyzing devices differently with respect to the FIB etched sample and second, by teaching the reworking of the FIB etched sample into a configuration that is suitable for analysis.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hitachi with that of Hirose'971 because a smaller separated sample can be inserted into various kinds of analyzing devices differently with respect to

sample 2 or the FIB sample may be re-etched into an optimal shape for observation and analysis,

Hirose'971 and Hitachi fail to teach the beam is an argon ion beam.

Mizumura teaches the beam is an argon ion beam (column 9, lines 26-35), with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Mizumura with that of Hirose'971 and Hitachi because the focus ion beam using argon has with the advantage of the ion beam can be irradiated onto a sample such as a silicon wafer without causing contamination of the sample with heavy metals.

Regarding claim 44, Hirose'971 teaches the first focused energy beam is a focused ion beam (column 4, line 48).

Regarding claim 46, Hirose'971 and Hitachi fail to teach the step of forming the sample chip with a rectangular parallelepiped shape in an asymmetric form to facilitate identification of the wall surface of the sample chip in the fourth step.

However, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 39, 42, and 45 rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose"971, Hitachi, and Mizumura as applied to claims 38, 41, and 43 above, and further in view of Chung et al, US Patent 5,604,156.

Regarding claim 39, Hirose'971, Hitachi, and Mizumura fail to teach the first step includes the step of processing the sample chip to form the wall surface having stepped portions due to differences in etching rate of materials forming in the wall surface of the sample chip.

However, at the time the invention of the instant application was made, it was well known in the art that etching at least two different materials with different etch rates results in a protrusion portion occurring on the surface of an area that is etched. An example of such is shown in Chung, figure 1E and column 2, lines 8-17, which teaches a stepped protrusion "C" occurring on the side wall surface of a trench due to the different etch rates of the semiconductor materials involved.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a stepped portion due to the difference in etching rates of materials forming the wall surface because this is an inherent feature that occurs when the semiconductor materials used have different etch rates.

Regarding claim 42, Hirose'971, Hitachi, and Mizumura fail to teach the first step and/or fifth step includes the step of processing the sample chip to form the wall surface having stepped portions due to differences in etching rate of materials forming in the wall surface of the sample chip.

However, at the time the invention of the instant application was made, it was well known in the art that etching at least two different materials with different etch rates results in a protrusion portion occurring on the surface of an area that is etched. An example of such is shown in Chung, figure 1E and column 2, lines 8-17, which teaches

a stepped protrusion "C" occurring on the side wall surface of a trench due to the different etch rates of the semiconductor materials involved.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a stepped portion due to the difference in etching rates of materials forming the wall surface because this is an inherent feature that occurs when the semiconductor materials used have different etch rates.

Regarding claim 45, Hirose'971, Hitachi, and Mizumura fail to teach the first step and/or fifth step includes the step of processing the sample chip to form the wall surface having stepped portions due to differences in etching rate of materials forming the wall surface of the sample chip.

However, at the time the invention of the instant application was made, it was well known in the art that etching at least two different materials with different etch rates results in a protrusion portion occurring on the surface of an area that is etched. An example of such is shown in Chung, figure 1E and column 2, lines 8-17, which teaches a stepped protrusion "C" occurring on the side wall surface of a trench due to the different etch rates of the semiconductor materials involved.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a stepped portion due to the difference in etching

rates of materials forming the wall surface because this is an inherent feature that occurs when the semiconductor materials used have different etch rates.

Response to Arguments

1. Applicant's arguments with respect to claims 1, 37, 39, 42, and 45 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed May 25, 2007, with regards to claims 36, 38, 40, 41, 43, 44, and 46 have been fully considered but they are not persuasive.

3. With regards to claims 36, 40, and 43, Applicant argues "... in order to further distinguish from the combined teachings of Hirose '971 and Hitachi. More specifically, each of amended independent claims 36, 40 and 43 recites a third step of irradiating a wall surface of the sample chip with an argon ion beam to thereby etch the wall surface. No corresponding step is disclosed or suggested by the combined teachings of Hirose'971 and Hitachi.... with respect to the use of an argon ion beam recited in dependent claims 38, 41 and 44, now the subject matter of amended independent claims 36, 40 and 43, respectively, the Examiner cited Mizumura for its teaching of employing an argon ion beam as the focused energy beam because an argon ion beam can be irradiated onto a sample (e.g., a silicon wafer) without causing contamination of the sample with heavy metals. However, Mizumura does not disclose or suggest the

irradiation of a wall surface (i.e., etching the wall surface) of a sample chip with an argon ion beam (third step) after the sample from which the sample chip is formed has been processed (i.e., has been irradiated) with a focused energy beam (first step), as recited in each of independent claims 36, 40 and 43".

4. In response to this argument, Mizumura teaches the use of several different types of focused ion beams that may be used with the present invention, with one of said focused beams having an argon gas source. An example of such beam is an argon gas field ionization ion source, called an Ar-FIS, which is discussed in column 27 of the third embodiment, Further, figure 47 of Mizumura shows that a focused ion beam taught in the invention are also used to further machine workpieces, such as a sample chip, by showing an irradiation of a workpiece surface to etch the surface in order to flatten the surface of the workpiece. Therefore, the reference of Mizumura does indeed teach that an argon ion beam is used for etching surfaces of a sample chip.

5. Therefore, the rejection of claims 36, 38, 40, 41, 43, and 44 as unpatentable under 35 USC 103(a) using the references of Hirose'971, Hitachi, and Mizumura is deemed proper.

Conclusion

Applicant's amendment (of **claims 1, 37, 39, 42, and 45 only)** necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

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PRIMARY PATENT EXAMINER